ABSTRACT OF THE DISCLOSURE

A method is provided for forming an improved planar structure of a semiconductor integrated circuit, and an integrated circuit formed according to the same. A field oxide is grown across the integrated circuit patterned and etched to form an opening with substantially vertical sidewalls exposing a portion of an upper surface of a substrate underlying the field oxide where an active area will be formed. A gate electrode comprising a polysilicon gate electrode and a gate oxide are formed over the exposed portion of the substrate. The polysilicon gate has a height at its upper surface above the substrate at or above the height of the upper surface of the field oxide. The gate electrode preferably also comprises a silicide above the polysilicon and an oxide capping layer above the silicide. LDD regions are formed in the substrate adjacent the gate electrode and sidewall spacers are formed along the sides of the gate electrode including the silicide and the capping layer.